IN THE CLAIMS:

Please amend claims 6, 17, 18, 22, 26 and 32 as follows:

1. (Original) A clock control system for generating a clock signal having an operating frequency set to a first frequency corresponding to a first junction temperature, comprising:

a thermal sensor operative to detect a junction temperature corresponding to at least a portion of a circuit on a die; and

a temperature dependent dynamic overclock generator circuit, operatively coupled to the thermal sensor, and operative to increase the operating frequency of the clock signal above the first frequency to at least one of: a second frequency corresponding to a second junction temperature and a third frequency corresponding to a third junction temperature, when the detected junction temperature is less than at least one of the second junction temperature and the third junction temperature, such that the second junction temperature and the third junction temperature is less than the first junction temperature.

2. (Original) The clock control system of claim 1 wherein the temperature dependent dynamic overclock generator circuit provides hysteresis based frequency control to increase the operating frequency of the clock signal above the first frequency to at least one of the second frequency and the third frequency if the detected junction temperature is below a lower junction temperature threshold, and the temperature dependent dynamic overclock generator circuit decreases the operating frequency of the clock signal below at least one of the second overclock frequency and the third overclock frequency to the first frequency if the

detected junction temperature is above an upper junction temperature threshold wherein the upper junction temperature threshold is greater than the lower junction temperature threshold.

3. (Original) The clock control system of claim 1 wherein the first junction temperature is a maximum rated junction temperature of at least the portion of the circuit on the die.

4. (Original) The clock control system of claim 1 wherein the temperature dependent dynamic overclock generator circuit dynamically varies the frequency of the clock signal between the first frequency and at least one of the second frequency and the third frequency over a transition time period.

5. (Original) The clock control system of claim 1 wherein the temperature dependent dynamic overclock generator circuit reduces at least one of: the frequency of the clock signal and a supply voltage to at least the portion of the circuit on the die if the detected junction temperature is above a junction temperature threshold.

6. (Currently Amended) A clock control system for generating a clock signal having an operating frequency set to a first frequency corresponding to a first junction temperature, comprising:

a thermal sensor operative to detect a junction temperature corresponding to at least a portion of a circuit on a die; and

a temperature dependent dynamic overclock generator circuit, operatively coupled to the thermal sensor, and operative to increase the operating frequency of the clock signal above the nominal operating frequency, when the detected junction temperature is [above] <u>below</u> the maximum rated junction temperature.

7. (Original) The clock control system of claim 6 wherein the temperature dependent dynamic overclock generator circuit further includes:

a clock generator circuit operative to produce the clock signal; and

temperature dependent dynamic overclock control logic, operatively coupled to the thermal sensor and operative to receive the temperature signal; and operatively coupled to the clock generator circuit, and operative to provide dynamic overclock frequency control data to the clock generator circuit in response to the received temperature signal to increase the operating frequency of the clock signal above the nominal operating frequency when the detected junction temperature is less than the maximum rated junction temperature.

8. (Original) The clock control system of claim 7 wherein the temperature dependent dynamic overclock control logic is operative to provide hysteresis based frequency control to: increase the operating frequency of the clock signal above the nominal operating frequency if the detected junction temperature is below a lower junction temperature threshold, and to decrease the operating frequency of the clock signal below the nominal operating frequency if the detected junction temperature is above an upper junction temperature threshold wherein the upper junction temperature threshold is greater than the lower junction temperature threshold.

9. (Original) The clock control system of claim 7 wherein the temperature dependent dynamic overclock control logic is operative to cause the clock generator circuit to increase the operating frequency of the clock signal above the nominal operating frequency such that the detected junction temperature does not exceed a threshold junction temperature.

10. (Original) The clock control system of claim 7 wherein the temperature dependent dynamic overclock control logic is operative to vary the operating frequency of the clock signal over a transition time period.

11. (Original) The clock control system of claim 7 wherein the temperature dependent dynamic overclock control logic is operative to reduce at least one of: the operating frequency of the clock signal and a supply voltage to at least the portion of the circuit on the die if the detected junction temperature is above a junction temperature threshold.

12. (Original) A clock control system for generating a clock signal having an operating frequency set to a nominal operating frequency corresponding to a maximum rated junction temperature, comprising:

a thermal sensor operative to produce a temperature signal corresponding to a junction temperature of at least a portion of a circuit on a die;

a thermal sensor control circuit, operatively coupled to the thermal sensor, and operative to produce temperature data in response to the temperature signal;

a clock generator circuit operative to produce the clock signal; and

a dynamic overclock frequency control data generator, operatively coupled to the thermal sensor control circuit and operative to receive the temperature data, and operatively coupled to the clock generator circuit, and operative to provide dynamic overclock frequency control data to the clock generator circuit in response to the received temperature data to cause the clock generator circuit to increase the operating frequency of the clock signal above the nominal operating frequency, when the detected junction temperature is less than the maximum rated junction temperature.

13. (Original) The clock control system of claim 12 wherein the dynamic overclock frequency control data generator is operative to provide hysteresis based frequency control to increase the operating frequency of the clock signal above the nominal operating frequency if the detected junction temperature is below a lower junction temperature threshold, and the temperature dependent dynamic overclock generator circuit decreases the operating frequency of the clock signal below the nominal operating frequency if the detected junction temperature is above an upper junction temperature threshold wherein the upper junction temperature threshold is greater than the lower junction temperature threshold

14. (Original) The clock control system of claim 12 wherein the thermal sensor control circuit further comprises:

an analog to digital converter, operatively coupled to the thermal sensor, and operative to produce the temperature data in response to the temperature signal; and

an interrupt control circuit, operatively coupled to the analog to digital converter, and operative to provide an interrupt control signal to the dynamic overclock frequency control data generator in response to the temperature data.

15. (Original) The clock control system of claim 14 wherein the interrupt control circuit is operative to produce the interrupt control signal in response to a comparison between the temperature data and the threshold temperature data, such that the dynamic overclock frequency control data generator is operative to produce the dynamic overclock frequency control data in response to the interrupt control signal.

16. (Original) The clock control system of claim 12 wherein the dynamic overclock frequency control data generator is operative to reduce at least one of: the frequency of the clock

signal and a supply voltage to at least the portion of the circuit on the die if the first junction temperature is above a junction temperature threshold.

17. (Currently Amended) A method for generating a clock signal having an operating frequency set to a nominal operating frequency corresponding to a maximum rated junction temperature, the method comprising:

detecting a junction temperature corresponding to at least a portion of a circuit on a die; and

increasing the operating frequency of the clock signal above the nominal operating frequency, when the detected junction temperature is [above] below the maximum rated junction temperature.

18. (Currently Amended) The method of claim 18 further including decreasing the operating frequency of the clock signal below the nominal operating frequency when the detected junction temperature is [below] above the maximum rated junction temperature.

19. (Original) The method of claim 18 further including providing hysteresis based frequency control by:

decreasing the operating frequency of the clock signal if the detected junction temperature is above an upper junction temperature threshold, and

increasing the operating frequency of the clock signal if the detected junction temperature is below a lower junction temperature threshold wherein the upper junction temperature threshold is greater than the lower junction temperature threshold.

20. (Original) A method for generating a clock signal having an operating frequency set to a first frequency corresponding to a first junction temperature, the method comprising:

detecting a junction temperature corresponding to at least a portion of a circuit on a die; and

increasing the operating frequency of the clock signal above the first frequency to at least one of a second frequency corresponding to a second junction temperature and a third frequency corresponding to a third junction temperature, when the detected junction temperature is less than at least one of: the second junction temperature and the third junction temperature, such that second junction temperature and the third junction temperature is less than the first junction temperature.

21. (Original) The method of claim 20 further including providing hysteresis based frequency control by:

decreasing the operating frequency of the clock signal if the detected junction temperature is above an upper junction temperature threshold, and

increasing the operating frequency of the clock signal if the detected junction temperature is below a lower junction temperature threshold wherein the upper junction temperature threshold is greater than the lower junction temperature threshold.

22. (Currently Amended) The method of claim 21 further including:

selecting a new upper junction temperature threshold and a new lower junction temperature threshold that is greater than the upper junction temperature threshold if the detected junction temperature is above the upper junction temperature threshold, and

selecting the new upper junction temperature threshold and [a] the new lower junction temperature threshold that is lower than the lower junction temperature threshold if the detected junction temperature is below the lower junction temperature threshold.

23. (Original) The method of claim 20 wherein the first junction temperature is a maximum rated junction temperature of at least the portion of the circuit on the die and the corresponding first frequency is a nominal operating frequency of the clock signal.

24. (Original) The method of claim 20 wherein increasing the operating frequency of the clock signal occurs over a transition time period such that as the operating frequency is increasing, the clock signal includes at least one intermediate frequency.

25. (Original) The method of claim 20 further comprising reducing at least one of: the frequency of the clock signal, and a supply voltage to at least the portion of the circuit on the die, if the detected junction temperature is above a junction temperature threshold.

26. (Currently Amended) A method for generating a clock signal having an operating frequency comprising:

detecting a junction temperature corresponding to at least a portion of a circuit on a die;

decreasing the operating frequency of the clock signal from a first frequency to a second frequency and selecting a new upper junction temperature threshold and a new lower junction temperature threshold that is higher than an upper junction temperature threshold if the detected junction temperature is above the upper junction temperature threshold; and

increasing the operating frequency of the clock signal from the first frequency to a third frequency and selecting the new higher upper junction temperature threshold and the [a] new lower junction temperature threshold that is lower than a lower junction temperature threshold if the detected junction temperature is below the lower junction temperature threshold.

27. (Original) The method of claim 26 further including producing an interrupt control signal if the detected junction temperature is at least one of: below the lower junction temperature threshold, and above the upper junction temperature threshold.

28. (Original) The method of claim 26 wherein increasing and decreasing the operating frequency of the clock signal occurs over a transition time period such that increasing and decreasing the operating frequency of the clock signal includes at least one intermediate frequency.

29. (Original) The method of claim 26 further comprising reducing at least one of: the frequency of the clock signal, and a supply voltage to at least the portion of the circuit on the die, if the detected junction temperature is above a maximum junction temperature threshold.

30. (Original) A method for generating a clock signal having an operating frequency set to a nominal operating frequency corresponding to a maximum rated junction temperature, the method comprising:

detecting a junction temperature corresponding to at least a portion of a circuit on a die;

increasing the operating frequency of the clock signal to a first frequency above the nominal operating frequency, when the detected junction temperature is less than a first junction temperature associated with the first frequency, such that the first junction temperature is less than the maximum rated junction temperature; and

increasing the operating frequency of the clock signal to a second frequency above the first frequency, when the detected junction temperature is less than a second junction temperature associated with the second frequency, such that the second junction temperature is less than the first junction temperature.

31. (Original) The method of claim 28 wherein increasing the operating frequency of the clock signal occurs over a transition time period such that as the operating frequency is increasing, the clock signal includes at least one intermediate frequency.

32. (Currently Amended) A memory containing instructions executable by one or more processing devices that causes the one or more processing devices to:

detect a junction temperature corresponding to at least a portion of a circuit on a die;

increase an operating frequency of a clock signal associated with at least the portion of the circuit on the die above a nominal operating frequency corresponding to a maximum rated junction temperature, when the detected junction temperature is [above] below the maximum rated junction temperature.

33. (Original) The memory of claim 32 containing executable instructions that causes the one or more processing devices to:

decrease the operating frequency of the clock signal if the detected junction temperature is above an upper junction temperature threshold; and

increase the operating frequency of the clock signal if the detected junction temperature is below a lower junction temperature threshold.